



13054
125-01

520.40524X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): T. KAWAHARA ET AL.
Serial No.: 09/932,099
Filed: August 20, 2001
For: SEMICONDUCTOR DEVICE
Group: 2811

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TC 2600 MAIL ROOM

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & §1.98

Assistant Commissioner of Patents
Washington, D.C. 20231

November 27, 2001

Sir:

In the matter of the above-identified application, Applicants are submitting herewith a documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted before the mailing date of a first office action on the merits.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

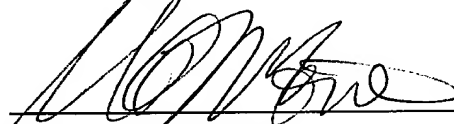
The relevance of the documents listed on the attached form equivalent to Form PTO-1449 is satisfied by the discussion of these documents in the specification (37 CFR §1.98(a)(3)).

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (520.40524X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Gregory E. Montone
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Sheet 1 of 1

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
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ATTY. DKT. NO.

SERIAL NO.

520.40524X00

09/932,099

INFORMATION DISCLOSURE STATEMENT
BY APPLICANT

(Use several sheets if necessary)

APPLICANT

T. KAWAHARA ET AL.

FILING DATE

GROUP

August 20, 2001

2811

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
	AA					
	AB					
	AC					
	AD					
	AE					
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	AH					
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FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation/Abstract	
						Yes	No
	AM						
	AN						
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AU	IEEE Micro, "Design Challenges of Technology Scaling", Vol. 19, No. 4, pp. 23-29, 1999
AV	IEEE SPECTRUM, "Identifying Defects in Deep-Submicron CMOS ICS", pp. 66-71, September, 1996
AW	Symposium on VLSI Circuits Digest of Technical Papers, "Subthreshold-Current Reduction Circuits for Multi-Gigabit DRAMS", pp. 45-46, May 1993
AX	ISSCC Digest of Technical Papers, "50% Active-Power Saving without Speed Degradation Using Standby Power Reduction (SPR) Circuit", pp. 318-319, 1995.
AY	Extended Abstract of the 1999 International Conference on Solid State Devices and Materials, "Suppression of Stand-by Tunnel Current in Ultra-Thin Gate Oxide MOSFETS", pp. 264-265, 1999

Examiner

Date Considered



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